ODD SEM LESSSON PLAN(SEM3, SEM5)

Faculty Name: Deepika Panda
Sem: 3rd
Subject: Digital Electronics
Academic Year: 2023-24
Duration: 1st Aug 2023 to 30th Nov 2023

WEEKS	No. of Days/per week Class allotted: **4**		Syllabus To be Covered
1ST WEEK	**Unit - 1 : Basics of Digital Electronics [12 Period]**		
	1st	1	Number System-Binary, Octal, Decimal, Hexadecimal
	2nd	2	Conversion from one system to another number system.
	3rd	3	Arithmetic Operation-Addition, Subtraction, Multiplication, Division
	4th	4	1's & 2's complement of Binary numbers& Subtraction using complements method
2ND WEEK	1st	5	Digital Code & its application & distinguish between weighted & non- weight Code, Binary codes, excess-3 and Gray codes.
	2nd	6	Logic gates: AND,OR,NOT,NAND,NOR, Exclusive-OR, Exclusive- NOR--Symbol, Function, expression, truth table & timing diagram
	3rd	7	Universal Gates & its Realisation
	4th	8	Universal Gates & its Realisation
3RD WEEK	1st	9	Boolean algebra, Boolean expressions, Demorgan's Theorems.
	2nd	10	Represent Logic Expression: SOP & POS forms
	3rd	11	Karnaugh map (3 & 4 Variables) & Minimization of logical expressions
	4th	12	Karnaugh map (3 & 4 Variables) don't care conditions
4TH WEEK	**Unit - 2: Combinational Logic Circuits [12 Period]**		
	1st	13	Half adder
	2nd	14	Full adder
	3rd	15	Half Subtractor
	4th	16	Full Subtractor
5TH WEEK	1st	17	Parallel Binary 4 bit adder.
	2nd	18	Serial adder
	3rd	19	Multiplexer (4:1)
	4th	20	De- multiplexer (1:4)
6TH WEEK	1st	21	Decoder, Encoder
	2nd	22	Digital comparator (3 Bit)
	3rd	23	Seven segment Decoder

	4th	24	Seven segment Decoder
7TH WEEK	**Unit-3: Sequential logic Circuits [12 Period]**		
	1st	25	Principle of flip-flops operation, its Types,
	2nd	26	Principle of flip-flops operation, its Types,
	3rd	27	SR Flip Flop using NAND Latch (un clocked)
	4th	28	SR Flip Flop using NOR Latch (un clocked)
8TH WEEK	1st	29	Clocked SR flip-flops-Symbol, logic Circuit, truth table and applications
	2nd	30	Clocked D flip-flops-Symbol, logic Circuit, truth table and applications
	3rd	31	Clocked JK flip-flops-Symbol, logic Circuit, truth table and applications
	4th	32	Clocked T flip-flops-Symbol, logic Circuit, truth table
			and applications
9TH WEEK	1st	33	Clocked JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
	2nd	34	Clocked JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
	3rd	35	Concept of Racing and how it can be avoided.
	4th	36	Concept of Racing and how it can be avoided.
10TH WEEK	**Unit-4: Registers, Memories & PLD [08 Period]**		
	1st	37	Shift Registers-Serial in Serial -out, Serial- in Parallel-out
	2nd	38	Shift Registers-Parallel in serial out and Parallel in parallel out
	3rd	39	Universal shift registers-Applications. Types of Counter & applications
	4th	40	Binary counter, Asynchronous ripple counter (UP & DOWN)
11TH WEEK	1st	41	Binary counter : Decade counter. Synchronous counter, Ring Counter.
	2nd	42	Binary counter : Ring Counter.
	3rd	43	Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM
	4th	44	Basic concept of PLD & applications
12TH WEEK	**Unit-5: A/D and D/A Converters [07 Period]**		
	1st	45	Necessity of A/D and D/A converters.
	2nd	46	D/A conversion using weighted resistors methods.
	3rd	47	D/A conversion using weighted resistors methods.
	4th	48	D/A conversion using R-2R ladder (Weighted resistors) network.
13TH WEEK	1st	49	D/A conversion using R-2R ladder (Weighted resistors) network.
	2nd	50	A/D conversion using counter method.
	3rd	51	A/D conversion using Successive approximate method
	Unit-6: LOGIC FAMILIES [09 Period]		

	4th	52	Various logic families & categories according to the IC fabrication process
14TH WEEK	1st	53	Various logic families & categories according to the IC fabrication process
	2nd	54	Characteristics of Digital ICs- Propagation Delay, fan-out, fan-in with Reference to logic families.
	3rd	55	Characteristics of Digital ICs- Power Dissipation, Noise
			Margin with Reference to logic families.
	4th	56	Characteristics of Digital ICs- Power Supply requirement with Reference to logic families.
15TH WEEK	1st	57	Characteristics of Digital ICs- Speed with Reference to logic families.
	2nd	58	Features, circuit operation & various applications of TTL (NAND)
	3rd	59	Features, circuit operation & various applications of CMOS (NAND)
	4th	**60**	Features, circuit operation & various applications of CMOS (NOR)

Faculty Name: Deepika Panda
Sem: 5th
Subject: VLSI AND EMBEDDED SYSTEMS(Th-3)
Academic Year: 2023-24
Duration: 1st Aug 2023 to 30th Nov 2023

Week	Class Day		Theory Topic
1ST			**1. Introduction to VLSI & MOS Transistor**
	1st	**1.1**	Historical perspective- Introduction
	2nd	**1.2**	Classification of CMOS digital circuit types
	3rd	1.3	Introduction to MOS Transistor& Basic operation of MOSFET.
	4th	1.4	Structure and operation of MOSFET (n-MOS enhancement type) & CMOS
2ND	**1st**	1.5	MOSFET V-I characteristics.
	2nd	**1.6**	Working of MOSFET capacitances.
	3rd	**1.7**	Modelling of MOS Transistors including Basic concept the SPICE level-1 models, the level-2 and level-3 model.
	4th	**1.8**	Flow Circuit design procedures
3RD	**1st**	**1.9**	VLSI Design Flow & Y chart
	2nd	**1.10**	Design Hierarchy
	3rd	**1.11**	VLSI design styles-FPGA, Gate Array Design, Standard cells based, Full custom
	4th	**1.11**	VLSI design styles-FPGA, Gate Array Design, Standard cells based, Full custom
4TH			2. **Fabrication of MOSFET**
	1st	**2.1**	Simplified process sequence for fabrication
	2nd	**2.2**	Basic steps in Fabrication processes Flow
	3rd	**2.3**	Fabrication process of nMOS Transistor

	4th	**2.4**	CMOS n-well Fabrication Process Flow
5TH	**1st**	**2.5**	MOS Fabrication process by n-well on p-substrate
	2nd	**2.5**	MOS Fabrication process by n-well on p-substrate
	3rd	**2.6**	CMOS Fabrication process by P-well on n-substrate
	4th	**2.6**	CMOS Fabrication process by P-well on n-substrate
6TH	**1st**	**2.7**	Layout Design rules
	2nd	**2.8**	Stick Diagrams of CMOS inverter
			3. **MOS Inverter**
	3rd	**3.1**	Basic NMOS inverters
	4th	**3.2**	Working of Resistive-load Inverter
7TH	**1st**	**3.2**	Working of Resistive-load Inverter
	2nd	**3.3**	Inverter with n-Type MOSFET Load – Enhancement Load, Depletion n-MOS inverter
	3rd	**3.3**	Inverter with n-Type MOSFET Load – Enhancement Load, Depletion n-MOS inverter
	4th	**3.4**	CMOS inverter – circuit operation and characteristics and interconnect effects: Delay time definitions
8TH	**1st**	**3.4**	CMOS inverter – circuit operation and characteristics and interconnect effects: Delay time definitions
	2nd	**3.5**	CMOS Inventor design with delay constraints – Two sample mask lay out for p-type substrate
	3rd	**3.5**	3.5 CMOS Inventor design with delay constraints – Two sample mask lay out for p-type substrate
			4. **Static Combinational, Sequential, Dynamics logic circuits & Memories**
	4th	**4.1**	Define Static Combinational logic, working of Static CMOS logic circuits (Two-input NAND Gate)
9TH	**1st**	**4.2**	CMOS logic circuits (NAND2) Gate
	2nd	**4.3**	CMOS Transmission Gates (Pass gate)
	3rd	**4.3**	CMOS Transmission Gates (Pass gate)
	4th	**4.4**	Complex Logic Circuits - Basics
10TH	**1st**	**4.5**	Classification of Logic circuits based on their temporal behaviour
	2nd	**4.6**	SR Flip latch Circuit
	3rd	**4.6**	SR Flip latch Circuit
	4th	**4.7**	Clocked SR latch only.
11TH	**1st**	**4.7**	Clocked SR latch only.
	2nd	**4.8**	CMOS D latch.
	3rd	**4.9**	Basic principles of Dynamic Pass Transistor Circuits
	4th	**4.10**	Dynamic RAM, SRAM
12TH	**1st**	**4.10**	Dynamic RAM, SRAM
	2nd	**4.11**	Flash memory
			5. **System Design method & synthesis**
	3rd	**5.1**	Design Language (SPL & HDL) & HDL & EDA tools & VHDL and packages Xilinx
	4th	**5.2**	Design strategies & concept of FPGA with standard cell-based design
13TH	**1st**	**5.3**	VHDL for design synthesis using CPLD or FPGA
	2nd	**5.4**	Raspberry Pi - Basic idea
			6. **Introduction to Embedded Systems**
	3rd	**6.1**	Embedded Systems Overview, list of embedded systems, characteristics, example – A Digital Camera

	4th	**6.1**	Embedded Systems Overview, list of embedded systems, characteristics, example – A Digital Camera
14TH	**1st**	**6.2**	Embedded Systems Technologies--Technology – Definition -Technology for Embedded Systems -Processor Technology -IC Technology
	2nd	**6.2**	Embedded Systems Technologies--Technology – Definition -Technology for Embedded Systems -Processor Technology -IC Technology
	3rd	**6.3**	Design Technology-Processor Technology, General Purpose Processors – Software, Basic Architecture of Single Purpose Processors – Hardware
	4th	**6.3**	Design Technology-Processor Technology, General Purpose Processors – Software, Basic Architecture of Single Purpose Processors – Hardware
15TH	**1st**	**6.4**	Application – Specific Processors, Microcontrollers, Digital Signal processors (DSP)
	2nd	**6.5**	IC Technology- Full Custom / VLSI, Semi-Custom ASIC (Gate Array & Standard Cell), PLD (Programmable Logic Device)
	3rd	**6.5**	IC Technology- Full Custom / VLSI, Semi-Custom ASIC (Gate Array & Standard Cell), PLD (Programmable Logic Device)
	4th	**6.6**	Basic idea of Arduino micro controller